WHAT IS CLAIMED IS:

1. A method of operating a memory circuit, comprising the steps of:

applying a first control signal to a gate of a memory cell transistor;

applying a second control signal pulse having a first edge and a second edge to the memory cell, the second edge having a maximum rate of change of voltage with respect to time that is smaller in magnitude than a maximum rate of change of voltage with respect to time of the first edge; and

accessing the memory cell in response to the first and second control signals.

2. A method as in claim 1, wherein the nonvolatile memory cell is a ferroelectric memory cell.

3. A method as in claim 2, wherein the nonvolatile memory cell comprises Lead Zirconate Titanate (PZT).

4. A method as in claim 2, wherein the nonvolatile memory cell comprises Strontium Bismuth Titanate (SBT).

5. A method as in claim 1, wherein the first control signal is a wordline signal, and wherein the second control signal is a plateline signal.

6. A method as in claim 1, wherein the step of accessing comprises one of reading and writing a datum from the memory cell.

7. A method as in claim 1, wherein the second control signal pulse comprises a third edge adjacent the second edge, the third edge having a maximum rate of change of voltage with respect to time that is different in magnitude than the maximum rate of change of voltage with respect to time of the second edge.

8. A memory circuit, comprising:

a memory cell for storing data, the memory cell having a first and a second control terminal;

a pass transistor having a control gate coupled to the first control terminal;

a first transistor of a first conductivity type having a current path coupled to the second control terminal and arranged to produce a first edge of a pulse; and

a second transistor of a second conductivity type having a current path coupled to the second control terminal and arranged to produce a second edge of the pulse, the second edge having a maximum rate of change of voltage with respect to time that is smaller in magnitude than a maximum rate of change of voltage with respect to time the first edge.

9. A memory circuit as in claim 8, wherein the memory cell is a ferroelectric memory cell.

10. A memory circuit as in claim 8, wherein the first control terminal is a wordline terminal.

11. A memory circuit as in claim 8, wherein the second control terminal is a plateline terminal.

12. A memory circuit as in claim 8, comprising a third transistor of the second conductivity type having a current path coupled to the second control terminal, the second and third transistor arranged to produce a third edge of the pulse adjacent the second edge.

13. A memory circuit as in claim 8, comprising a third transistor of the second conductivity type having a current path coupled to the second control terminal, the third transistor having a greater width-to-length ratio than the second transistor, the third transistor arranged to produce a third edge of the pulse adjacent the second edge.

14. A memory circuit, comprising:

a memory cell for storing data, the memory cell having a first and a second control terminal;

a pass transistor having a control gate coupled to the first control terminal;

a first transistor of a first conductivity type having a current path coupled to the second control terminal and arranged to produce at least one of a first edge of a first pulse and a first edge of a second pulse;

a second transistor of a second conductivity type having a current path coupled to the second control terminal and arranged to produce a second edge of the first pulse and a second edge of the second pulse; and

a third transistor of the second conductivity type having a current path coupled to the second control terminal and arranged to produce the second edge of the first pulse.

15. A memory circuit as in claim 14, wherein the memory cell is a ferroelectric memory cell.

16. A memory circuit as in claim 14, wherein the first control terminal is a wordline terminal and the second control terminal is a plateline terminal.

17. A memory circuit as in claim 14, wherein the second edge of the second pulse has a maximum rate of change of voltage with respect to time that is smaller in magnitude than a maximum rate of change of voltage with respect to time of the first edge of the second pulse.

18. A memory circuit as in claim 14, wherein the second edge of the second pulse has a maximum rate of change of voltage with respect to time that is smaller in magnitude than a maximum rate of change of voltage with respect to time of the second edge of the first pulse.

19. A memory circuit as in claim 14, wherein the second and a third transistor produce a third edge of the second pulse adjacent the second edge of the second pulse.

20. A memory circuit as in claim 14, wherein a third transistor produces a third edge of the second pulse adjacent the second edge of the second pulse, the third transistor having a greater width-to-length ratio than the second transistor.

21. A method of operating a memory circuit, comprising the steps of:

applying a first control signal to a first terminal of a memory cell;

applying a first pulse to a second terminal of the memory cell, the first pulse having a first edge and a second edge; and

applying a second pulse to the second terminal, the second pulse having a first edge and a second edge, the second edge having a maximum rate of change of voltage with respect to time that is smaller in magnitude than a maximum rate of change of voltage with respect to time of the second edge of the first pulse.

22. A method as in claim 21, wherein the memory cell is a ferroelectric memory cell.

23. A method as in claim 21, wherein the first control terminal is a wordline terminal and the second control terminal is a plateline terminal.

24. A method as in claim 21, wherein the second pulse comprises a third edge adjacent the second edge, the third edge having a maximum rate of change of voltage with respect to time that is different in magnitude than a maximum rate of change of voltage with respect to time of the second edge of the second pulse.

25. A method of operating a memory circuit, comprising the steps of:

applying a first control signal to a first terminal of a memory cell;

applying a first pulse to a second terminal of the memory cell, the first pulse having a first edge and a second edge; and

applying a second pulse to the second terminal, the second pulse having a first edge and a second edge, the second edge having a maximum rate of change of voltage with respect to time that is smaller in magnitude than a maximum rate of change of voltage with respect to time of the first edge of the second pulse.

26. A method as in claim 25, wherein the memory cell is a ferroelectric memory cell.

27. A method as in claim 25, wherein the first control terminal is a wordline terminal and the second control terminal is a plateline terminal.

28. A method as in claim 25, wherein the second pulse comprises a third edge adjacent the second edge, the third edge having a maximum rate of change of voltage with respect to time that is different in magnitude than a maximum rate of change of voltage with respect to time of the second edge of the second pulse.

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